REMARKS

Claims 1, 3-5, 9-46, and 51-82 have been amended. No new claims have been added. Claims 84-88 have been canceled. Claims 1, 3-5, 9-46, and 51-83 are pending.

Claim 42 stands objected to due to a minor informality. Claim 42 has been amended to address the objection noted in the Office Action. Accordingly, the objection to claim 42 should be withdrawn.

Claims 1-3, 7-11, 21-24, and 33-34 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Perino (U.S. Patent No. 6,426,984). The remaining claims are rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino in view of one or more secondary references. More specifically:

claims 4-5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino in view of Co (U.S. Patent No. 6,584,576);

claims 12-14 and 29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino in view of Yamagishi (U.S. Patent No. 6,336,190);

claims 15-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino in view of Magro (U.S. Patent No. 6,516,362);

claims 30-32 and 35-36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino in view of Yamagishi and Magro;

claim 37 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino in view of Yamagishi, Magro, and Mizukami (U.S. Patent No. 5,422,858);

claims 38-41 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino in view of Gillingham (U.S. Patent No. 6,510,503);

claims 25-28, 42-43, 46, 48-51, 68, 72-73, and 87-72 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino in view of Gasbarro (U.S. Patent No. 5,432,823);

claims 69-71 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino in view of Gasbarro and Gillingham;

claims 52-67 and 75-77 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino in view of Gasbarro, Gillingham, and Magro; and

claim 74 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino in view of Gasbarro and Yamagishi.

These rejections are respectfully traversed.

Claim 1 recites, *inter alia*, "said predetermined location is at approximately a mid point of a plurality of spaced locations each adapted to accept a device, and supply said device with said first and second clock signals, said predetermined phase relationship is substantially an in-phase relationship, said first and second clock signals are independent signals, one of said first and second clock signals is a data write clock signal, and the other of said first and second clock signals is a data read clock signal."

Claim 42 recites, *inter alia*, "said predetermined location is at approximately a mid point of a plurality of spaced locations each adapted to accept a device, and supply said device with said first and second clock signals, such that when said first and second clock signals are received at one of said plurality of spaced locations, a predetermined minimum time equal to at least about half a clock period of one of said first or second clock signals exists before said first and second clock signals are received at another one of said plurality of spaced locations, said first and second clock signals

are independent signals, one of said first and second clock signals is a data write clock signal, and the other of said first and second clock signals is a data read clock signal."

Claim 68 recites, *inter alia*, "a memory controller coupled to said bus for respectively issuing said data write and data read clock signals on said data write and data read clock signal paths and for setting a predetermined phase relationship between said data write and data read clock signals at a predetermined location along said bus, said predetermined location being at approximately a mid point of a plurality of spaced locations each adapted to accept a device, and supply said device with said data write clock and data read clock signals."

Claim 83 recites, *inter alia*, "said memory controller setting a phase relationship between said data write and data read clock signals at said predetermined location which ensures that at any one of said memory subsystems a data read operation is not initiated following initiation of a data write operation during a time period which is equal to about 50% of the period of a data bit time."

Referring to Fig. 5, Perino discloses a system 70 comprising a master device 24 and a plurality of slave devices 26A, 26B, ... 26N. The master device can communicate with the slave devices 26A-26N using two clock signals CLOCK1, CLOCK2 generated by a clock generator 72. As the length of the paths 28, 30 which carry the clock signals CLOCK1, CLOCK2 are different, there is a phase difference between the two clock signals CLOCK1, CLOCK2. Perino discloses sensing the clock signals at nodes A, B, detecting the phase difference between the two clock signals CLOCK1, CLOCK2 at nodes A, B, and adjusting the CLOCK2 signal until the two clock signals CLOCK1, CLOCK2 are essentially in-phase at nodes A, B.

As seen in Fig. 5, nodes A, B is located between the master 24 and the first slave device 26A. In an alternate embodiment as illustrated in Fig. 7, delay devices 136A, 136B can be place in series with nodes A, B to effectively monitor the phase difference existing inside the first slave device 26A (i.e., at virtual nodes A', B').

Perino further discloses yet another alternate embodiment, wherein the phase difference between the two clock signals CLOCK1, CLOCK2 are not minimized at any point. Instead, an amplifier 152 is used to boost the signal level of CLOCK2 so that CLOCK2 can be easily received at the first slave device 26A. See Fig. 10; Column 7, lines 23-25.

Perino is solely concerned about signal quality of the clock signals at or proximate to the first one of a plurality of slave devices (i.e., device 26A). In the embodiments illustrated by Figs. 5 and 7, Perino discloses how phase differences between the two clock signals CLOCK1, CLOCK2 can be minimized at or near the first slave device 26A by sampling the clock signals CLOCK1, CLOCK2 at nodes A, B, and adjusting the phase of the CLOCK2 signal. Significantly, the location where the phase differences are minimized is either at nodes A and B, or at virtual nodes A' and B'. Nodes A and B are near the slave device 26A, but on the side of the slave device 26A facing the master, while virtual nodes A' and B' coincide with the location of the slave device 26A. See column 7, lines 1-10 and Fig. 9, which shows a relatively small phase shift at device 26A, but large amounts of phase shifting at many of the other devices (e.g., 26B). (The other embodiment of Perino addresses signal strength, and is wholly irrelevant to the claimed invention.)

Perino therefore fails to disclose or suggest an apparatus or method which maintains a predetermined phase relationship between independent read and write clock signals at a predetermined location when that predetermined location is at (claims

1 and 42) or being (claim 68) "approximately a mid point of a plurality of spaced locations each adapted to accept a device," as recited in independent claims 1, 42, and 68.

Perino does not specifically disclose any minimum spacing between different devices. Accordingly, Perino further fails to disclose or suggest "said memory controller setting a phase relationship between said data write and data read clock signals at said predetermined location which ensures that at any one of said memory subsystems a data read operation is not initiated following initiation of a data write operation during a time period which is equal to about 50% of the period of a data bit time."

The Office Action additionally cites to Co, Yamagishi, Gasbarro, Gillingham, Mizukami and Magro. However, these references also do not disclose or suggest the above-recited portions of the independent claims 1, 42, 68, and 83.

Accordingly, claim 1, 42, 68, and 83 are therefore believed to be allowable over the prior art of record. The depending claims (i.e., claims 3-5, 9-41, 43-46, and 51-67, and 69-82) are also believed to be allowable for at least the same reasons as the independent claims.

Further, with respect to depending claims 4-5, claim 4 recites "configuring the signal propagation characteristics of at least one of said first and second conductive paths to obtain said predetermined relationship" and has been amended to depend from claim 3. The Office Action alleges that Co configuring propagation characteristics of a conductive path. It is respectfully asserted that this conclusion is in error.

Referring to Fig. 3, Co discloses a method of improving the clock-to-data timing (TQ) characteristics of multiple RDRAM memory devices 14-1, 14-2, 14-3 within

a RIMM memory module 10. More specifically, a first timing element 12 is inserted in series at one end of the RIMM module 10 on the clock-to-master line CTM, while a complementary timing element 16 is inserted in series on the other end of the RIMM module. The result of using the delay 12 and complementary delay 16 elements is to minimize the TQ parameter of the RIMM module, thereby permitting a system to include more RIMM modules. See column 2, lines 10-22. Co therefore discloses that it can be advantageous for the purpose of reducing a TQ parameter in a RIMM module to include a complementary pair of timing elements 12, 16, coupled in series with the clock-to-master line. Since the delay 12 and complementary delay devices 16 are part of the RIMM module, Co discloses a static (i.e., at time of manufacturing) method for affecting signal timing.

As claim 4 now depends from claim 3, which recite "detecting" and "adjusting" acts which are performed on an functional system. The steps recited in claims 4-5 therefore apply to the operation of altering the signal propagation characteristics on a functional system. This aspect of the invention is not disclosed or suggested by Co, which is directed to how a memory module may be designed to minimize the TQ parameter.

With respect to claims 12-14 and 29, these claims each recite features directed to regeneration of a clock signal. The Office Action alleges that it would have been obvious to include the clock regeneration feature disclosed by Yamagishi into the system of Perino to arrive at the claimed invention. It is respectfully asserted that this conclusion is in error.

Yamagishi discloses a high speed synchronous memory device. Referring to Fig. 1, it can be seen that the memory device 1 accepts a basic clock signal which drives a PLL 3. The PLL 3 outputs a signal to a clock generator 4 which generates a plurality

of internal clock signals. Each internal clock signal is routed into a respective storage element group 5a ... 5n, and drives a respective PLL 51a ... 51n. The PLL regenerates the clock signal and distributes it to individual storage elements. One of the storage elements 5n also routes the output of its PLL 51n to a PLL which regenerates the signal as a return clock signal to a clock tree circuit 7.

Yamagishi, therefore discloses a single clock system. Thus, Yamagishi does not disclose or suggest the use of read and write clock signals. Additionally, since each of the clock signals in the storage apparatus 1 is a PLL synchronized version of the basic clock signal, none of the clock signals can be said to be an independent signal. It is respectfully asserted that the signal clock system of Yamagishi is fundamentally different from dual clock system of Perino, and therefore it would not have been obvious to combine the references in the manner suggested in the Office Action.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Christopher S. Chow
Registration No.: 46,493
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant